IN THE CLAIMS

1. (Currently Amended) A method of programming in a non-volatile semiconductor memory device having a memory cell array formed of a plurality of cell strings each of which is connected through a first and second select transistor between a bit line and a common source line and each of which includes a plurality of cell transistors, formed in a pocket P-well, control gates of each memory cell transistor being respectively coupled to a word line arranged in parallel between a first and second select line, the method comprising the steps of:

~~performing~~ during a bit line setup operation, applying ~~in which~~ one of a first and a second ~~voltages, the second voltage being lower than the first voltage, is applied~~ voltage to the bit lines corresponding to the cell strings in accordance with data bits to be programmed, the second voltage being lower than the first voltage, and biasing the first select line to the first voltage; ~~and~~

during a string select line setup operation after the bit line setup operation, biasing the first select line to a third voltage between the first voltage and the second voltage; and

~~performing~~ during a programming operation after the string select line setup operation, applying ~~in which~~ a program voltage ~~is applied~~ to a selected one of the word lines~~,~~ ~~wherein~~

~~the first select line is biased to the second voltage during a first time in the bit line setup operation and is biased to a third voltage between the first voltage and the second voltage during a second time after the bit line set up operation~~.

2. (Currently Amended) The method of claim 1, wherein the first voltage is a ~~ground~~ power supply voltage and the second voltage is a ~~power supply~~ ground voltage.

3. (Original) The method of claim 1, wherein the third voltage is sufficient to turn on the first select transistor connected to the bit line corresponding to a data bit to be programmed.

4. (Original) The method of claim 1, wherein the third voltage is between a fourth and fifth voltage, wherein the fourth voltage is sufficient to turn on the first select transistor connected to the bit line corresponding to the data bit to be programmed, and the fifth voltage is a shut-off voltage of the first select transistor for the bit line corresponding to

the data bit to be program inhibited, the shut-off voltage being determined by the first voltage – (β x Vpgm), wherein β is a coupling ratio of the word line to the string select line, and wherein Vpgm is the program voltage.

5. (Original) The method of claim 1, wherein the third voltage is a voltage corresponding to a threshold voltage of a N-channel metal oxide semiconductor (NMOS) transistor or to a sum of the threshold voltages of plural NMOS transistors.

6. (Currently Amended) The method of claim 1, wherein the ~~first time is sufficient~~ bit line setup operation is long enough to raise the bit line corresponding to a data bit to be programmed to the first voltage.

7. (Currently Amended) The method of claim 1, wherein the ~~second time is~~ string select line setup operation occurs in an interval between completion of the bit line setup operation and completion of a program operation.

8. (Original) The method of claim 1, wherein the bit line corresponding to the data bit to be program inhibited is electrically isolated from the cell string corresponding thereto after the bit line setup operation, and a channel voltage of a memory cell transistor, connected to a select word line, corresponding to the data bit to be program inhibited is self-boosted higher than the first voltage when the program voltage is applied to the select word line.

9. (Original) The method of claim 8, wherein the self-boosting operation includes a local self-boosting operation.

10. (Original) The method of claim 9, wherein the self-boosting operation is achieved by applying a pass voltage to the unselect word line and by applying the ground voltage to the unselect word line adjacent to the select word line before applying the program voltage to the select word line.

11. (Original) The method of claim 9, wherein the self-boosting operation is achieved by applying a pass voltage to the unselect word line and by applying the ground

voltage to the two unselect word lines adjacent to the select word line before applying the program voltage to the select word line.

12. (Original) The method of claim 9, wherein the self-boosting operation is achieved by applying a first pass voltage to all the word lines and by concurrently applying the program voltage and a second pass voltage to the select and unselect bit lines, wherein the first pass voltage is lower than the second pass voltage.

13. (Original) The method of claim 9, wherein the self-boosting operation is achieved by applying a first pass voltage to all the word lines, by applying a second pass voltage higher than the first pass voltage to the unselect word line, and by applying the ground voltage to the unselect word line adjacent to the select word line before applying the program voltage to the select word line.

14. (Original) The method of claim 9, wherein the self-boosting operation is performed by applying a first pass voltage to all the word lines, by applying a second pass voltage higher than the first pass voltage to the unselect word line, and by applying the ground voltage to the two unselect word lines adjacent to the select word line before applying the program voltage to the select word line.

15. (Original) The method of claim 1, wherein the bit line corresponding to the data bit to be program inhibited is electrically isolated from the cell string corresponding thereto after the bit line setup operation, and wherein a pass voltage lower than the program voltage is applied to the unselect word lines for a channel voltage of memory cell transistors of the cell string corresponding to the program inhibit data bit to be self-boosted when the program voltage is applied to the select word line.

16. (Original) A method of programming in a non-volatile semiconductor memory device having a memory cell array formed of a plurality of cell strings each of which is connected through a first and second select transistors between a bit line and a common source line and has a plurality of cell transistors, formed in a pocket P-well, having control gates of the memory cell transistor being respectively coupled to a word line arranged in parallel between a first and second select line, method comprising the steps of:

applying one of a first and second voltage, the second voltage being lower than the first voltage, to the bit lines corresponding to the cell strings in accordance with the data bits to be programmed, in such manner that the first select line is biased to the first voltage;

biasing the first select line to a third voltage that is between the first voltage and the second voltage; and

applying a program voltage to a selected one of the word lines, in such manner that the first select line is biased to the third voltage.

17. (Currently Amended) The method of claim 16, wherein the first voltage is a ~~ground~~ power supply voltage, and the second voltage is a ~~power supply~~ ground voltage.

18. (Original) The method of claim 16, wherein the third voltage is sufficient to turn on the first select transistor connected to the bit line corresponding to the data bit to be programmed.

19. (Original) The method of claim of 16, wherein the third voltage is between a fourth and fifth voltage, wherein the fourth voltage is sufficient to turn on the first select transistor connected to the bit line corresponding to the data bit to be programmed, and wherein the fifth voltage is a shut-off voltage of the first select transistor for the bit line corresponding to the data bit to be program inhibited, the shut-off voltage being determined by the first voltage – (β x Vpgm), wherein β is a coupling ratio of the word line to the string select line, and wherein Vpgm is the program voltage.

20. (Original) The method of claim 16, wherein the third voltage is a voltage corresponding to a sum of threshold voltages of one or more NMOS transistors.

21. (Currently Amended) A non-volatile semiconductor memory device comprising:

a memory cell array having a plurality of cell strings formed of a string select transistor having a drain connected to a bit line corresponding thereto, a ground select transistor having a source connected to a common source line, and a plurality of memory cell transistors serially connected between a source of the string select transistor and a drain of the ground select transistor, word lines connected to control gates of the memory cell transistors in the respective cell string, a string select line commonly connected to gates of the string

select transistors in the respective cell string, and a ground select line commonly connected to gates of the ground select transistors in the respective cell string;

a means for controlling potentials of the select lines and the word lines in accordance with a bit line setup period, string select line setup period, a program period, and a discharge period of a program cycle; and

a page buffer circuit for supplying a first and second voltage to the bit lines in accordance with the data bits to be programmed in the memory cell array during the bit line setup period of the program cycle,

wherein the control means biases the string select line to the first voltage during the bit line setup period and to a third voltage between the first and second voltages during the string select line setup and program periods.

22. (Currently Amended) The device of claim 21, wherein the first voltage is a ~~ground~~ power supply voltage, and the second voltage is a ~~power supply~~ ground voltage.

23. (Original) The device of claim 21, wherein the third voltage is sufficient to turn on the string select transistor connected to the bit line corresponding to the data bit to be programmed.

24. (Original) The device of claim 21, wherein the third voltage is between a fourth and fifth voltages, wherein the fourth voltage is sufficient to turn on the first select transistor connected to the bit line corresponding to the data bit to be programmed, and wherein the fifth voltage is a shut-off voltage of the first select transistor for the bit line corresponding to the data bit to be program inhibited, the shut-off voltage being determined by the first voltage – (β x Vpgm), wherein β is a coupling ratio of the word line to the string select line and wherein Vpgm is the program voltage.

25. (Original) The device of claim 21, wherein the third voltage is substantially twice a threshold voltage of NMOS transistor.

26. (New) A method of programming in a non-volatile semiconductor memory device having a memory cell array formed of a plurality of cell strings each of which is connected through a first and second select transistor between a bit line and a common source line and each of which includes a plurality of cell transistors, formed in a pocket P-well,

control gates of each memory cell transistor being respectively coupled to a word line arranged in parallel between a first and second select line, the method comprising the steps of:

performing a bit line setup operation in which one of first and second voltages, the second voltage being lower than the first voltage, is applied to the bit lines corresponding to the cell strings in accordance with data bits to be programmed; and

performing a programming operation in which a program voltage is applied to a selected one of the word lines,

wherein the first select line is biased to the first voltage during a first time in the bit line setup operation and is biased to a third voltage between the first voltage and the second voltage during a second time after the bit line set up operation, wherein the third voltage is between a fourth and fifth voltage, wherein the fourth voltage is sufficient to turn on the first select transistor connected to the bit line corresponding to the data bit to be programmed, and the fifth voltage is a shut-off voltage of the first select transistor for the bit line corresponding to the data bit to be program inhibited, the shut-off voltage being determined by the first voltage – (β x Vpgm), wherein β is a coupling ratio of the word line to the string select line, and wherein Vpgm is the program voltage.

27. (New) A method of programming in a non-volatile semiconductor memory device having a memory cell array formed of a plurality of cell strings each of which is connected through a first and second select transistors between a bit line and a common source line and has a plurality of cell transistors, formed in a pocket P-well, having control gates of the memory cell transistor being respectively coupled to a word line arranged in parallel between a first and second select line, method comprising the steps of:

applying one of a first and second voltage, the second voltage being lower than the first voltage, to the bit lines corresponding to the cell strings in accordance with the data bits to be programmed, in such manner that the first select line is biased to the first voltage;

biasing the first select line to a third voltage that is between the first voltage and the second voltage; and

applying a program voltage to a selected one of the word lines, in such manner that the first select line is biased to the third voltage, wherein the third voltage is between a fourth and fifth voltage, wherein the fourth voltage is sufficient to turn on the first select transistor connected to the bit line corresponding to the data bit to be programmed, and wherein the fifth voltage is a shut-off voltage of the first select transistor for the bit line corresponding to

the data bit to be program inhibited, the shut-off voltage being determined by the first voltage – (β x Vpgm), wherein β is a coupling ratio of the word line to the string select line, and wherein Vpgm is the program voltage.

28. (New) A non-volatile semiconductor memory device comprising:

a memory cell array having a plurality of cell strings formed of a string select transistor having a drain connected to a bit line corresponding thereto, a ground select transistor having a source connected to a common source line, and a plurality of memory cell transistors serially connected between a source of the string select transistor and a drain of the ground select transistor, word lines connected to control gates of the memory cell transistors in the respective cell string, a string select line commonly connected to gates of the string select transistors in the respective cell string, and a ground select line commonly connected to gates of the ground select transistors in the respective cell string;

a means for controlling potentials of the select lines and the word lines in accordance with a bit line setup, string select line setup, a program, and a discharge period of a program cycle; and

a page buffer circuit for supplying a first and second voltage to the bit lines in accordance with the data bits to be programmed in the memory cell array during the bit line setup period of the program cycle,

wherein the control means biases the string select line to the first voltage during the bit line setup period and to a third voltage between the first and second voltages during the string select line setup and program periods, wherein the third voltage is between a fourth and fifth voltages, wherein the fourth voltage is sufficient to turn on the first select transistor connected to the bit line corresponding to the data bit to be programmed, and wherein the fifth voltage is a shut-off voltage of the first select transistor for the bit line corresponding to the data bit to be program inhibited, the shut-off voltage being determined by the first voltage – (β x Vpgm), wherein β is a coupling ratio of the word line to the string select line and wherein Vpgm is the program voltage.

29. (New) A non-volatile semiconductor memory device comprising:

a memory cell array having a plurality of cell strings formed of a string select transistor having a drain connected to a bit line corresponding thereto, a ground select transistor having a source connected to a common source line, and a plurality of memory cell transistors serially connected between a source of the string select transistor and a drain of the

ground select transistor, word lines connected to control gates of the memory cell transistors in the respective cell string, a string select line commonly connected to gates of the string select transistors in the respective cell string, and a ground select line commonly connected to gates of the ground select transistors in the respective cell string;

a means for controlling potentials of the select lines and the word lines in accordance with a bit line setup, string select line setup, a program, and a discharge period of a program cycle; and

a page buffer circuit for supplying a first and second voltage to the bit lines in accordance with the data bits to be programmed in the memory cell array during the bit line setup period of the program cycle,

wherein the control means biases the string select line to the first voltage during the bit line setup period and to a third voltage between the first and second voltages during the string select line setup and program periods, wherein the third voltage is substantially twice a threshold voltage of a NMOS transistor.